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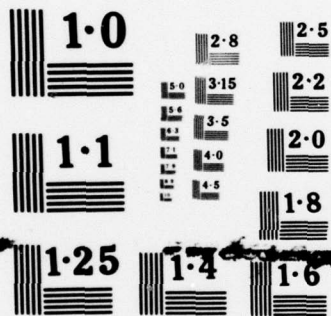
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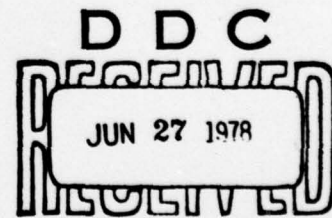
FLOATING DECK GRID MODULATOR

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MAY 1978

Second Interim Report for Period June 1977 to September 1977

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ABSTRACT

Both NPN and PNP driver circuits have been breadboarded and satisfactorily tested using a worst case transformer primary equivalent circuit load. The preliminary designs of the transformer and pulse top regulator have been completed.

SUMMARY

The transformer driver circuits provide 0.1 μ sec peak power pulses of approximately 1.5 kW and approximately 0.6 kW through the 10 μ sec pulse width. The breadboard circuit tests indicate that both the NPN and PNP circuits provide adequate current levels and rise times while operating within their specified voltage and power ratings.

The transformer windings have been fabricated and are ready for fitting of the copper tube end turns and core.

PROGRAM OBJECTIVE

This program effort is intended to develop a documented working model of a pulse transformer type TWT grid modulator (See Figure 1). This particular configuration has been chosen in order to minimize the amount of circuitry at the TWT cathode potential, and thus enhance reliability and maintainability. The pulse transformer secondary will drive the TWT grid directly while referenced to the -50 kV TWT cathode potential. The primary of the transformer is to be driven by solid state circuitry operating at potentials ranging from 200 to 400 volts with respect to chassis ground. The secondary output is to be a 2 kV pulse to modulate the grid of a high powered TWT.

PROGRAM ORGANIZATION

The design portion of the program is to be accomplished in three separate phases corresponding to the three major design problems associated with a modulator of this type.

1. The transformer must be able to withstand a secondary to primary voltage stress of -50 kV and simultaneously exhibit a primary leakage inductance low enough to allow a secondary pulse rise time of 1 μ sec maximum.
2. The primary drive transistors must be designed to operate at very high peak power dissipations at high temperatures without failures due to secondary breakdown. The primary drive circuitry must operate with current rise and fall times $<0.5 \mu$ sec to charge and discharge the circuit stray capacity.
3. Since the pulse transformer must be under damped to provide the short rise and fall times required, it will exhibit overshoot and ringing. The phase stability requirements of the TWT will therefore force regulation of the grid pulse top. Active circuitry must be designed to perform pulse top clipping and regulating functions and negative bias clamp functions.

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Existing, proven circuit designs will be used where possible to minimize design time. The PNP transformer drive circuitry, the pulse top clipper regulator, the TWT bias fault circuitry and the TWT filament fault circuitry all as designed for the AN/TPQ-36 system can be used with very minor modifications.

FLOATING DECK FUNCTIONS

Three different devices for primary drive circuits are under investigation; the PNP transistor, the NPN transistor and the gate turn-off (GTO) SCR. Preliminary circuit designs will be used to determine the optimum performance and most economical configuration.

The pulse top clipper regulator will be in the form of a closed control loop that both clips the oscillations on the modulator transformer secondary and controls the level of the TWT grid pulse across the width of the pulse.

Since interpulse negative grid voltage must only maintain the TWT in the off state and is not otherwise critical, the bias supply may be an unregulated transformer-rectifier power supply.

The clamp supply clamps the negative overshoot from the modulator transformer to a level within the rating of the TWT.

One secondary of the power isolation transformer provides power for the TWT heater regulator. The heater regulator then provides stable power at 8V and 10A to the TWT filament. The voltage from the other secondary of the power isolation transformer is rectified and filtered and used to supply regulated 30 Vdc to 80 kHz inverters which in turn provide power to the various circuit components on the floating deck.

The TWT filament fault circuit and the TWT grid bias fault circuit provide optical signals through fiber optic couplers from the -42 kV level to transmitter control unit (TCU) interfaces at ground level. If the TWT filament voltage drifts either high or low, the "heater OK" signal to the TCU is removed and system operation is terminated. If the TWT grid bias voltage drifts above a preset value, the "bias OK" signal to the TCU is removed and system operation is terminated.

FINANCIAL STATUS

Present contract funding appears to be adequate to successfully complete the task. Expenditures through the end of August are as follows:

Labor - 738 Manhours
Total - \$16.6K

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DESIGN REQUIREMENT OUTLINE

I. DRIVERS

- a. NPN
- b. PNP
- c. GTO SCR

II. MODULATOR TRANSFORMER

- a. IN/OUT Volt Levels
- b. Driving PNT Impedance (rise time)
- c. Size, Weight

III. PULSE TOP CLIPPER

- a. Amplifier
- b. Control Element (Transistor)
- c. Voltage Shifters (Zeners)
- d. Input Circuits (Sensors)

IV. BIAS SUPPLY

- a. Bias for Mod Transformer
- b. Negative Clamp

V. INSTRUMENTATION

- a. Filament Fault
- b. Bias Fault

VI. POWER SUPPLIES

- a. TWT Heater
- b. 30 Vdc
- c. 80 kHz Inverters

MODULATOR PERFORMANCE OBJECTIVES

| Parameter | Symbol | Design Goal |
|-------------------------|------------------|---------------------|
| Grid pulse rise time | t_r | $< 1 \mu\text{sec}$ |
| Grid pulse fall time | t_f | $< 1 \mu\text{sec}$ |
| Minimum Pulse width | T_w | $1 \mu\text{sec}$ |
| Maximum Pulse width | T_w | $10 \mu\text{sec}$ |
| Maximum duty cycle | D_{max} | 5% |
| Pulse top overshoot | V_{pk} | 10% |
| Pulse top Stability | ΔE | 0.0058% RMS max |

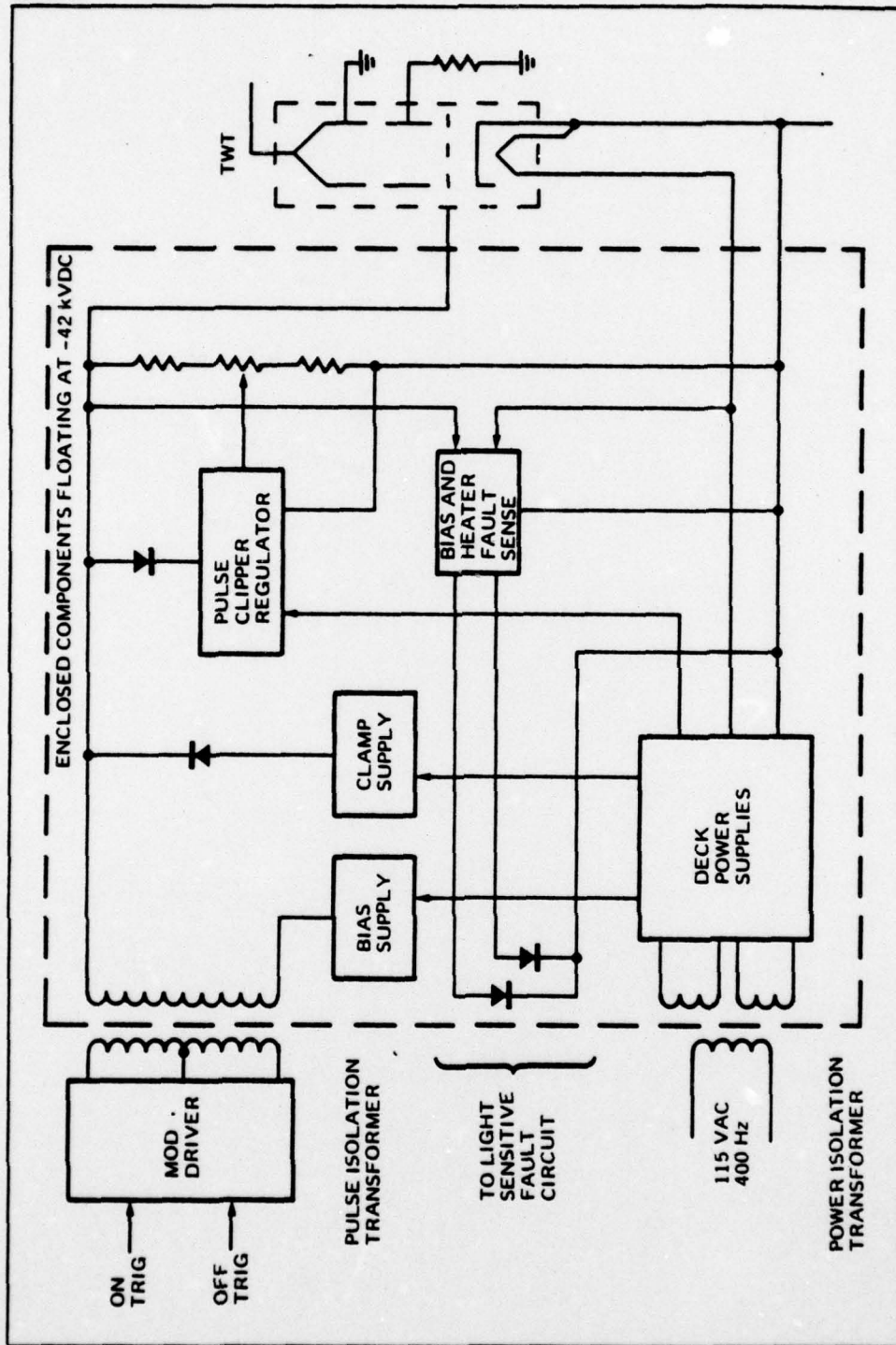


Figure 1. Floating Deck Block Diagram

PROGRESS

During the reporting period, the designs of the modulator transformer, driver circuits, and clipper regulator were completed. Details of these designs are as follows:

Modulator Transformer

The modulator transformer is constructed on a core of 2 mil 80% Ni. The core geometry and material were selected to provide a 10 μ sec pulse width with minimum pulse top droop. The transformer construction is shown in Figure 2. Each primary winding is made of 2 mil copper foil to achieve closer coupling and thus a lower leakage inductance. The secondary winding is No. 26 AWG magnet wire. The primary and secondary are insulated for a 50 kV voltage gradient with Kapton and Kraft paper. The start and finish turns of each of the secondary windings is made of 1/4" copper tubing to minimize the voltage gradient to the surrounding ground potential.

Driver Circuits

The PNP (Figure 3) and the NPN (Figure 4) driver circuits exhibit very similar operating characteristics in the modulator transformer equivalent test circuit of Figure 6. The circuit designs are identical with circuit implementation differing only in power supply and semiconductor polarity reversals. The output transistor is driven on by a fast pulse coupled through the 0.22 μ fd capacitor from the intermediate driver transistor. The output transistor is maintained in the on state for the remainder of the 10 μ sec pulse by the input pulse transformer. Two driver circuits are used to operate the modulator transformer; one as an "on" driver and one as an "off" driver.

The Gate Turn Off SCR (GTO) circuit (Figure 5) offers some circuit simplicity but the device is susceptible to gate leakage instability at higher temperatures. The GTO driver will be tested as time permits.

TYPICAL DRIVER CIRCUIT TEST RESULTS

| <u>Parameter</u> (See Fig. 6) | <u>Rise</u> <u>Time</u> | <u>Peak</u> <u>Value</u> | <u>Steady State Value</u> (10 μ sec Intrapulse Period) |
|----------------------------------|----------------------------|-----------------------------|---|
| V_O | 0.1 μ sec | 220 Volts | 0.5 Volts |
| i_L | 0.1 μ sec | 4 Amps | 3 Amperes |
| V_L | 0.4 μ sec | 200 Volts | \approx 200 Volts |

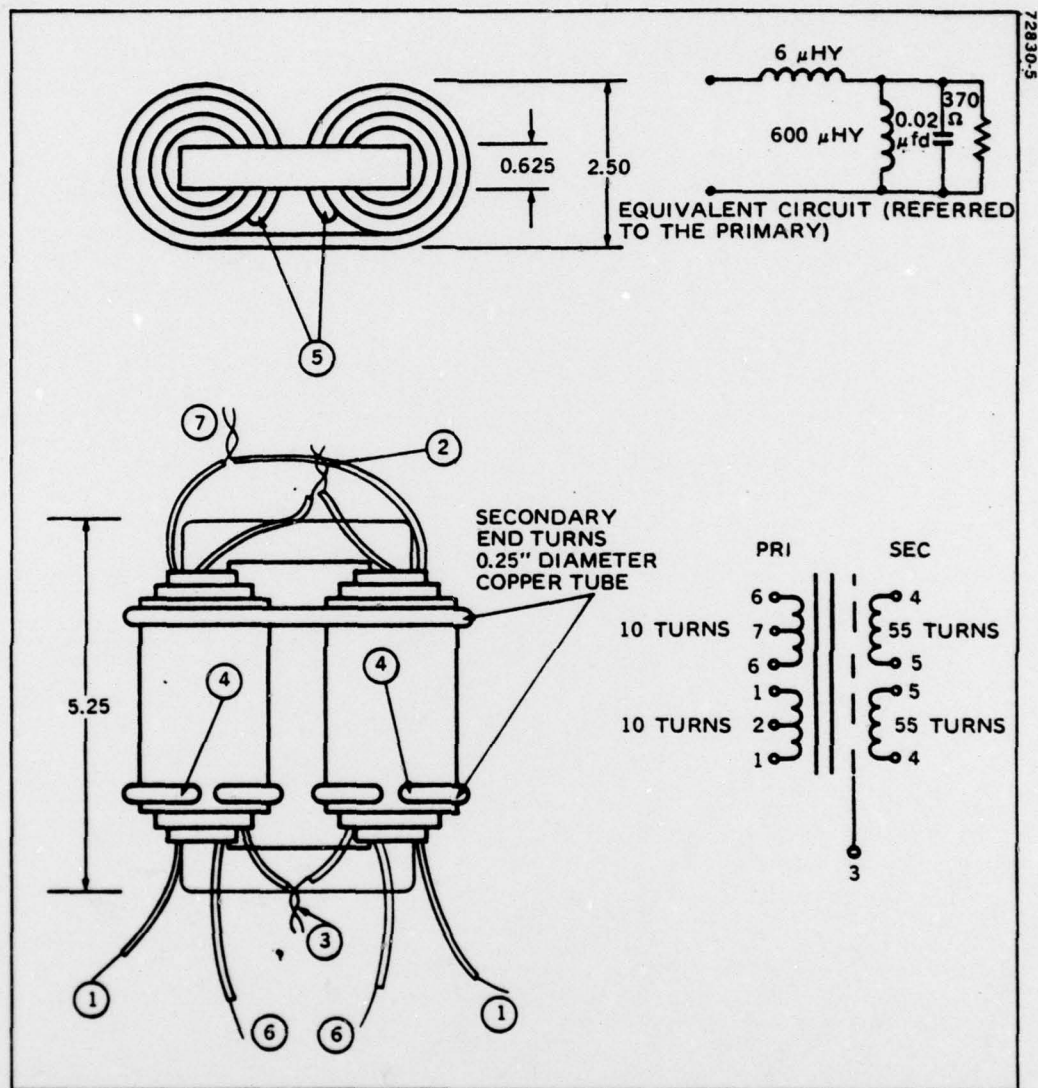
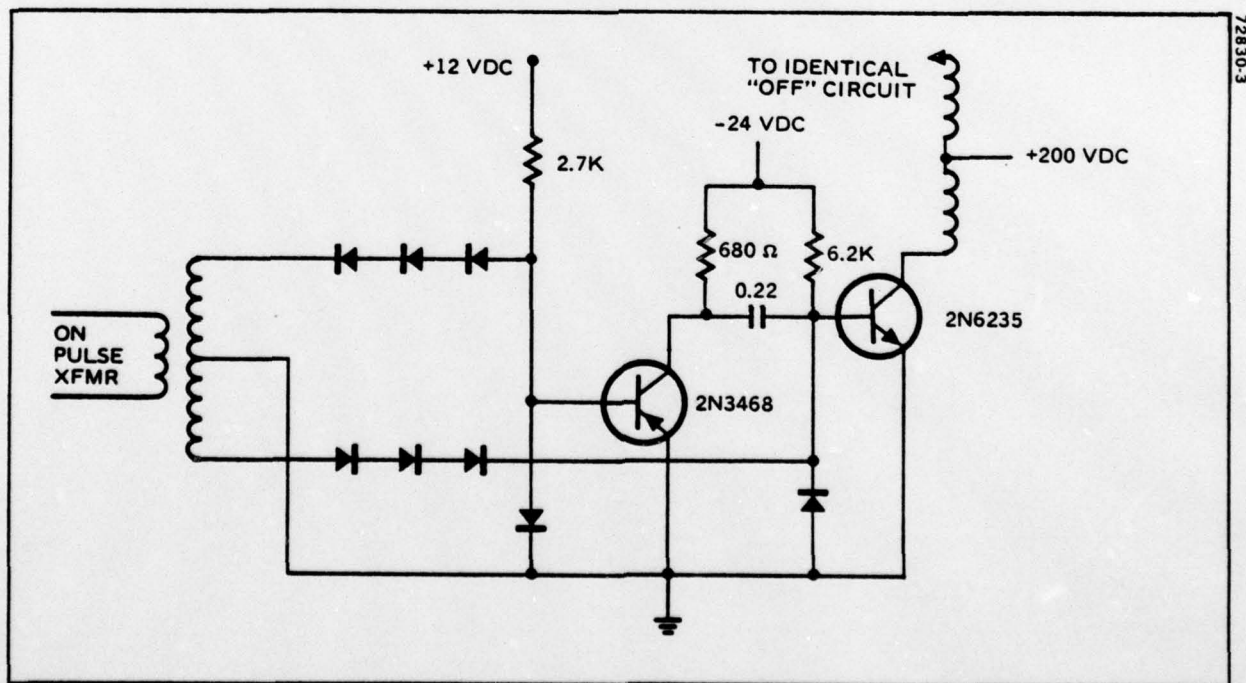
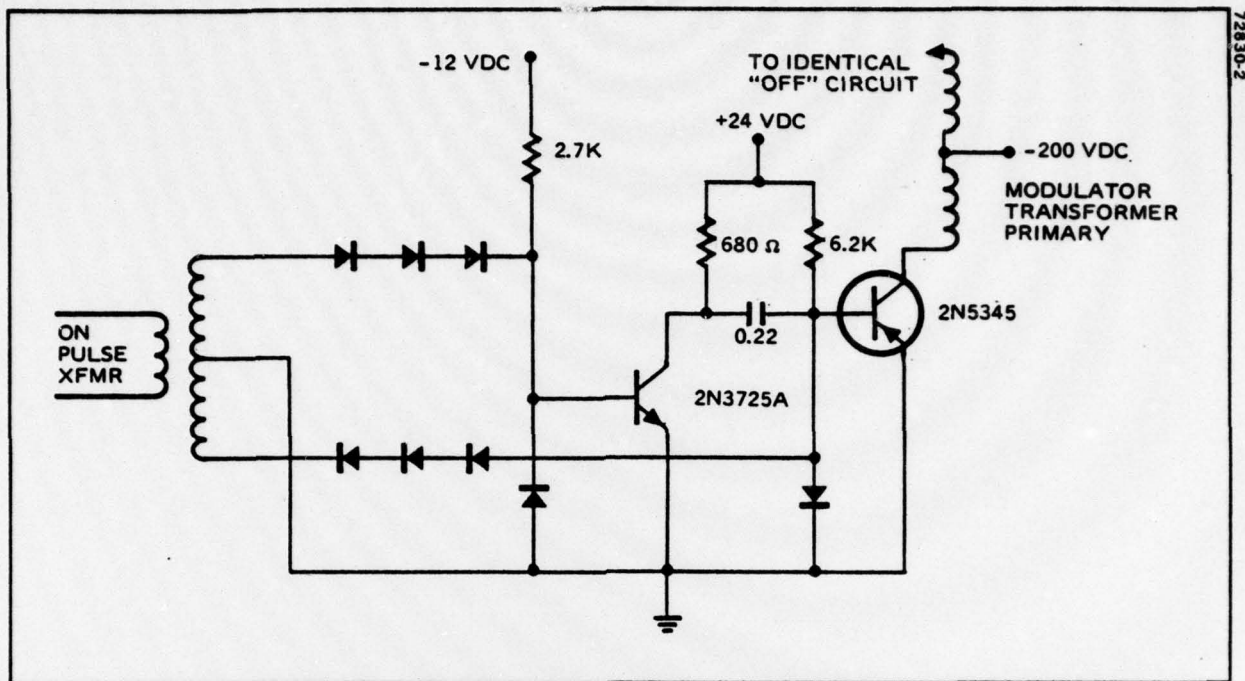


Figure 2. Modulator Transformer Construction



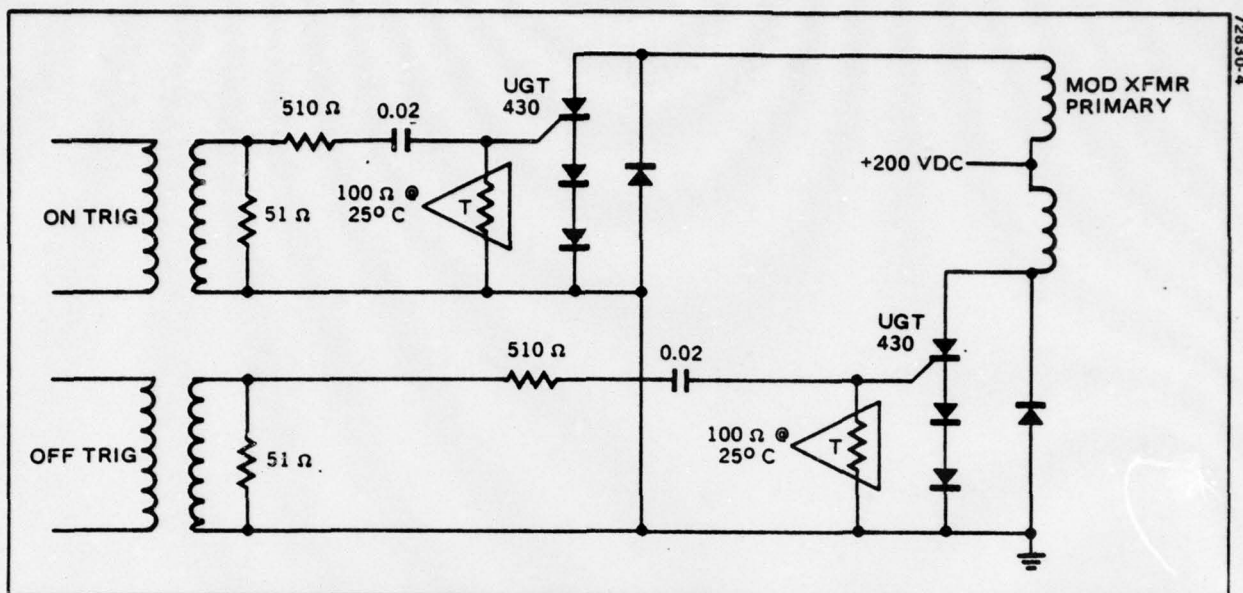


Figure 5. Gate Turn Off SCR Modulator Driver

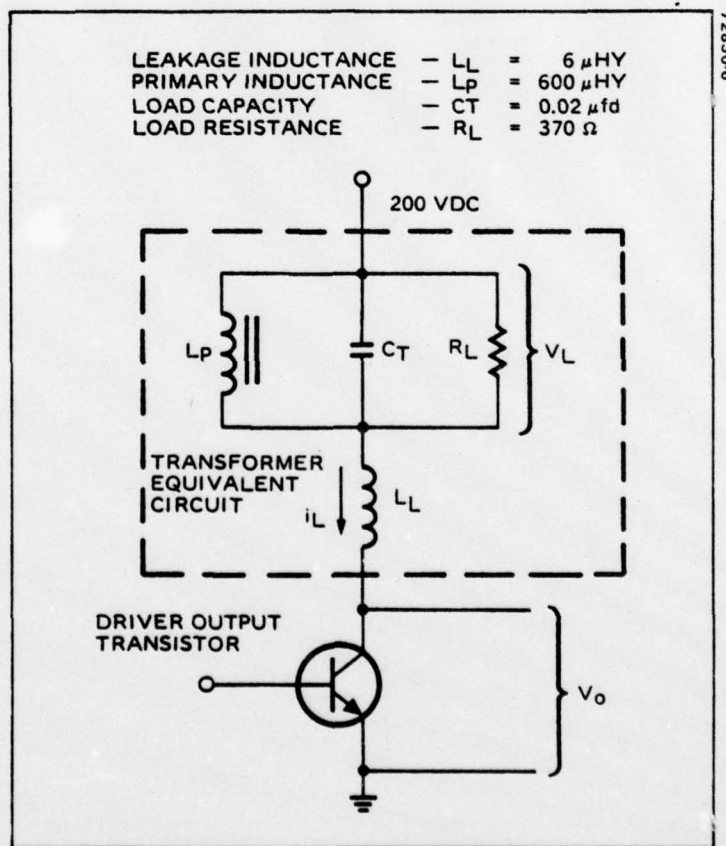


Figure 6. Modulator Transformer Equivalent Test Circuit

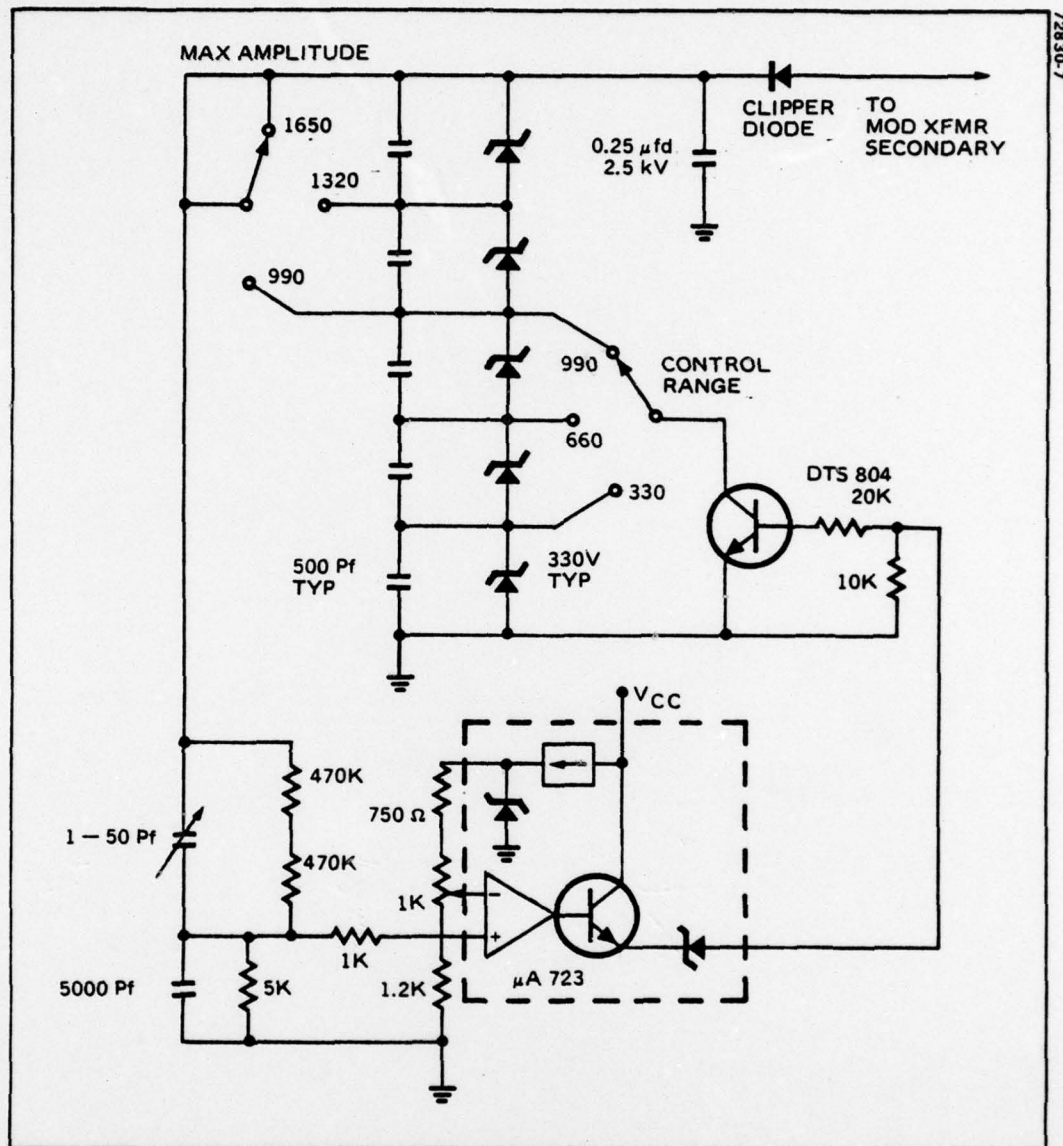


Figure 7. Pulse Top Clipper Regulator

Clipper Regulator Circuit

The clipper regulator circuit (Figure 7) maintains a constant positive voltage on the 0.25 μ fd clipper capacitor. The modulator transformer secondary positive excursion is thus limited to this level by the clipper diode. Voltage changes on the clipper capacitor are sensed by the compensated divider network, amplified and used to control the current through the DTS 804 and the series stack of 330 volt zener diodes. The zener diodes limit the collector voltage on the DTS 804 to a safe level (990 volts) and also bound the clipper control range between +1650 volts max and +660 volts min.

CONCLUSIONS

The driving point impedance of the transformer appears to be compatible with the proposed drive circuits. The transformer input parameters, as measured with the equivalent circuit, are reasonable and typical of this type of circuit. The circuit stresses are moderate and indicate that a conservative design is possible.

SUBSEQUENT PROGRAM DIRECTION

The transformer will be completed and tested, without high voltage stress, to ascertain its exact characteristics. The pulse top regulator and bias supply will be constructed and separately tested. After successful completion of the individual tests, the units will be interconnected and tested as a composite system.